IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) In a data processing system having a first component and a second component, the improvement comprising:

a. A first data bus having a first set of characteristics responsively coupled between said first component and said second component;

b. A second data bus ~~base~~ having a second set of characteristics responsively coupled between said first component and said second component; and

c. A circuit responsively coupled to said first data bus and said second data bus having a single set of interrupt handling logic and a selector for multiplexing transfers from said first data bus and said second data bus which combines said first data bus and said second data bus into a logical bus having a third set of characteristics wherein said third set of characteristics is different from either said first set of characteristics and said second set of characteristics.

2. (Original) A data processing system according to claim 1 wherein said first set of characteristics includes a first maximum transfer rate, said second set of characteristics includes a second maximum transfer rate, and said third set of characteristics includes a third maximum transfer rate and wherein said third maximum transfer rate is greater than either of said first maximum transfer rate and said second maximum transfer rate.

3. (Original) A data processing system according to claim 2 wherein said third maximum transfer rate is the sum of said first maximum transfer rate and said second maximum transfer rate.

4. (Original) A data processing system according to claim 3 wherein said first maximum transfer rate and said second maximum transfer rate are equal.

5. (Previously Presented) A data processing system according to claim 4 wherein said first maximum transfer rate is equal to 66 MHz.

6. (Currently Amended) A data processing system comprising:

a. A first component;

b. A second component;

c. A first data bus responsively coupled between said first component and said second component;

d. A second data bus responsively coupled between said first component and said second component; and

e. A circuit responsively coupled to said first data bus and said second data bus having a selector for multiplexing transfers from said first data bus and said second data bus which combines said first data bus and said second data bus into a logical bus.

7. (Original) A data processing system according to claim 6 wherein said first data bus has a first set of characteristics, said second data bus has a second set of characteristics, said logical bus has a third set of characteristics, and said third set of characteristics if different from said first set of characteristics and said second set of characteristics.

8. (Original) A data processing system according to claim 7 wherein said first set of characteristics includes a first data transfer rate, said second set of characteristics includes a second data transfer rate, said third set of characteristics includes a third data transfer rate, and said third data transfer rate is greater than either of said first data transfer rate and said second data transfer rate.

9. (Original) A data processing system according to claim 8 wherein said third data transfer rate equals the sum of said first data transfer rate and said second data transfer rate.

10. (Original) A data processing system according to claim 9 wherein said first data transfer rate is equal to said second data transfer rate.

11. (Currently Amended) A method of coupling a first component to a second component within a data processing system comprising:

a. Providing a first data bus having a first set of characteristics responsively coupled between said first component and said second component;

b. Providing a second data bus having a second set of characteristics responsively coupled between said first component and said second component; and

c. Combining said first data bus and said second data bus using a single set of interrupt handling logic from said first data bus and said second data bus to produce a logical bus having a third set of characteristics.

12. (Original) A method according to claim 11 wherein said first set of characteristics includes a first data transfer rate, said second set of characteristics includes a second data transfer rate, said third set of characteristics includes a third data transfer rate, and said third data transfer rate is greater than either of said first data transfer rate and said second data transfer rate.

13. (Original) A method according to claim 12 wherein said third data transfer rate is equal to the sum of said first data transfer rate and said second data transfer rate.

14. (Original) A method according to claim 13 wherein said first data transfer rate is equal to said second data transfer rate.

15. (Previously Presented) A method according to claim 14 wherein said first data transfer rate is equal to 66 MHz.

16. (Currently Amended) An apparatus comprising:

a. First performing means for performing a first data processing function;

b. Second performing means for performing a second data processing function;

c. First transferring means responsively coupled to said first performing means and said second performing means for transferring data from said first performing means to said second performing means in accordance with a first set of characteristics;

d. Second transferring means responsively coupled to said first performing means and said second performing means for transferring data from said first performing means to said second performing means in accordance with a second set of characteristics; and

e. Combining means responsively coupled to said first transferring means and said second transferring means for combining said first transferring means and said second transferring means into a logical transferring means having a third set of characteristics having a single set of interrupt handling logic and a selector for multiplexing transfers from said first data bus and said second data bus.

17. (Original) An apparatus according to claim 16 wherein said first set of characteristics includes a first transfer rate, said second set of characteristics includes a second transfer rate, said third set of characteristics includes a third transfer rate,

and said third transfer rate is greater than either of said first transfer rate and said second transfer rate.

18. (Original) An apparatus according to claim 17 wherein said third transfer rate equals the sum of said first transfer rate and said second transfer rate.

19. (Original) An apparatus according to claim 18 wherein said first transfer rate equals said second transfer rate.

20. (Previously Presented) An apparatus according to claim 19 wherein said first transfer rate is equal to 66 MHz.